REMARKS

Claims 1-5, 7 and 13-18 are pending in this application. By this Amendment, claims 1-5, 7 and 13-17 are amended. Various amendments are made for clarity and are unrelated to issues of patentability.

The Office Action rejects claims 1-3 and 13-18 under 35 U.S.C. §103(a) over Applicants Admitted Prior Art (hereafter AAPA) in view of U.S. Patent 5,876,536 to Kumar. The Office Action also rejects claims 4-7 under 35 U.S.C. §102(a) by AAPA. The rejections are respectfully traversed with respect to the pending claims.

Independent claim 1 recites a digital data receiver for receiving a digital video data signal and a synchronous signal, a digital video controller for supplying gamma-corrected digital video data signal to the digital data receiver and for supplying sustain pulse number information to the digital data receiver, a multi-chip module in which a plurality of control chips having a control circuit for controlling the PDP, and a plurality of memories are mounted on a single package on a single printed circuit board (PCB) of a control board separately from the digital data receiver and the digital video controller, and a plurality of buffers for buffering signals between the multi-chip module and a plurality of driving units. Independent claim 1 also recites that the multi-chip module includes a plurality of green tapes, and input/output (I/O) lines coupling the plurality of control chips and the plurality of memories are formed in the plurality of green tapes within the single package.

The applied references do not teach or suggest all the features of independent claim 1. More specifically, the Office Action asserts that the timing controller 32 (FIG. 3) of AAPA

corresponds to the claimed multi-chip module (MCM). Applicant respectfully disagrees. The timing controller 32 of FIG. 4 and MCM 62 (in FIG. 5, for example) are not the same at least for the following reasons.

FIG. 4 shows that a line pointed to by numeral 32 is a timing controller. This is merely for explanation. That is, the line pointed to by the numeral 32 is imaginary. The timing controller indicated by numeral 32 is a group of elements that are coupled by a large plurality of signal lines. See paragraph [0021] of the present specification. In contrast, FIG. 5 of the present specification shows that a MCM 62 is actually a single element and a single package in which a plurality of control chips and memories are formed.

FIG. 4 of the present specification shows that control chips 26 and memories 33 are mounted on the control board 13 together with the other elements, such as a digital data receiving part 31, a digital video controller 37 and buffers 34, 35, 36. However, in FIG. 5, control chips and memories are mounted on a single package separately from the other elements, such as a digital data receiving part 31, a digital video controller 37 and buffers 34, 35, 36.

AAPA does not teach or suggest a digital data receiver for receiving a digital video data signal and a synchronous signal, a digital video controller for supplying gamma-corrected digital video data signal to the digital data receiver and for supplying sustain pulse number information to the digital data receiver, a multi-chip module in which a plurality of control chips having a control circuit for controlling the PDP, and a plurality of memories are mounted on a single package on a single printed circuit board (PCB) of a control board separately from the digital

data receiver and the digital video controller. Kumar does not teach or suggest these features of independent claim 1 missing from AAPA.

Thus, AAPA and Kumar do not teach or suggest all the features of independent claim 1. Independent claim 1 therefore defines patentable subject matter.

Independent claim 4 recites a control board provided with a multi-chip module in which a plurality of control chips having a control circuit for controlling a plasma display panel (PDP), and a plurality of memories are mounted on a single package on a single printed circuit board of the control board, the multi-chip module including a plurality of green tapes, and input/output (I/O) lines coupling the plurality of control chips and the plurality of memories being formed in the plurality of green tapes within the single package. Independent claim 4 also recites that the control board comprises: a plurality of driving units for generating and applying a driving signal corresponding to a control signal generated from the control board, and the PDP for displaying an image by a plasma discharge according to the driving signal applied from each of the plurality of driving units. Independent claim 4 further recites that the control board comprises a digital data receiver for receiving a digital video data signal and a synchronous signal, a digital video controller for supplying gamma-corrected digital video data signal to the digital data receiver and for supplying sustain pulse number information to the digital data receiver, and a plurality of buffers for buffering signals between the multi-chip module and the plurality of driving units. Still further, independent claim 4 recites that the multi-chip module is mounted on the single printed circuit board separately from the digital data receiver and the digital video controller.

For at least similar reasons as set forth above, AAPA and Kumar do not teach or suggest all the features of independent claim 4. More specifically, AAPA (and Kumar) does not teach or suggest a control board provided with a multi-chip module in which a plurality of control chips having a control circuit for controlling a plasma display panel (PDP), and a plurality of memories are mounted on a single package on a single printed circuit board of the control board in combination with the control board comprises: a digital data receiver (for receiving a digital video data signal and a synchronous signal), a digital video controller (for supplying gamma-corrected digital video data signal to the digital data receiver and for supplying sustain pulse number information to the digital data receiver), and a plurality of buffers (for buffering signals between the multi-chip module and the plurality of driving units), and wherein the multi-chip module is mounted on the single printed circuit board separately from the digital data receiver and the digital video controller. Independent claim 4 therefore defines patentable subject matter.

Independent claim 13 recites a digital data receiver for receiving a digital video data signal and a synchronous signal, a digital video controller for supplying gamma-corrected digital video data signal to the digital data receiver and for supplying sustain pulse number information to the digital data receiver, a multi-chip module in which at least one of a plurality of control chips having a control circuit for controlling the PDP, and at least one memory of a plurality of memories are mounted on a single package on a single printed circuit board of a control board separately from the digital data receiver and the digital video controller, and a plurality of buffers for buffering signals between the multi-chip module and a plurality of driving units. Independent claim 13 also recites that the multi-chip module includes a circuit package having a plurality of

circuit layers, and wherein at least one of the plurality of control chips and at least one of the plurality of memories are formed on a front of the circuit package and input/output (I/O) lines are formed through the plurality of circuit layers, and the I/O lines connect the at least one control chip and the at least one memory within the single package.

For at least similar reasons as set forth above, AAPA and Kumar do not teach or suggest at least these features of independent claim 13. More specifically, AAPA (and Kumar) does not teach or suggest a digital data receiver (for receiving a digital video data signal and a synchronous signal), a digital video controller (for supplying gamma-corrected digital video data signal to the digital data receiver and for supplying sustain pulse number information to the digital data receiver), a multi-chip module in which at least one of a plurality of control chips having a control circuit for controlling the PDP, and at least one memory of a plurality of memories are mounted on a single package on a single printed circuit board of a control board separately from the digital data receiver and the digital video controller. Thus, independent claim 13 defines patentable subject matter.

For at least the reasons set forth above, each of independent claims 1, 4 and 13 defines patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In addition, the dependent claims recite features that further and independently distinguish over the applied references.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-5, 7 and 13-18 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
KED & ASSOCIATES, LLP

David C. Oren
Registration No. 38,694

P.O. Box 221200
Chantilly, Virginia 20153-1200
(703) 766-3777 DCO/kah
Date: February 17, 2009
Please direct all correspondence to Customer Number 34610